Next Generation Ferroelectric Memories enabled by Hafnium Oxide

T. Mikolajick1,2, U. Schroeder1, P. D. Lomenzo1, E. T. Breyer1, H. Mulaosmanovic1, M. Hoffmann1, T. Mittmann1, F. Mehmood1, B. Max2, and S. Slesazeck1

1NaMLab gGmbH, Noethnitzer Strasse 64 a, 01187 Dresden, Germany, email: thomas.mikolajick@namlab.com 2Institute of Semiconductors and Microsystems, TU Dresden, 01062 Dresden, Germany,

***Abstract*—**Ferroelectrics are theoretically an ideal solution for low write power nonvolatile memories. However, the complexity of ferroelectric perovskites has hindered the scaling of such devices to competitive feature sizes. The discovery of ferroelectricity in hafnium oxide solved this issue. Ferroelectric memories in three variants, capacitor based ferroelectric RAM, ferroelectric field effect transistors and ferroelectric tunneling junctions have become competitors for future memory solutions again. In this paper, the basics and current status of hafnium oxide based ferroelectric memory devices is described and recent results are shown.

**I.**  **INTRODUCTION**

Ferroelectrics are materials that show a remanent polarization that can be switched between two directions using an electrical field. The stable nonvolatile polarization paired with the purely field driven switching, make this class of materials a natural choice for nonvolatile memories overcoming the write inefficiency of most other emerging nonvolatile memory concepts [1]. However, typically the materials that show ferroelectricity have a complex structure with three or more compounds and in the case of oxides normally weakly bound oxygen (see fig. 1 b). These properties make them very hard to integrate into a state of the art CMOS process [2]. As a result, the established ferroelectric memory technologies are limited in scaling and therefore are only used in niche applications. Thus, after an intense phase of research and development between the late 1990s and the mid 2000s, the interest in ferroelectrics for memory applications diminished. The discovery of ferroelectricity in doped hafnium oxide (see fig. 1a) has changed that view since hafnium oxide is used as the gate dielectric in modern transistors since 2007. Traditionally, a 1 transistor – 1 capacitor cell (FeRAM see fig. 2a) inspired by DRAM is used in established ferroelectric memory devices. An alternative way is to integrate the ferroelectric into the gate stack of an MOS transistor (FeFET see fig. 2b). Finally, a resistive switching ferroelectric tunneling junction can be achieved when the ferroelectric is made very thin and allows for a polarization dependent tunneling current (FTJ see fig. 2c). All three memory concepts have seen increased activities by using hafnium oxide based ferroelectrics rather than traditional perovskites or layered perovskites.

**II.FERROELECTRICITY IN HAFNIUM OXIDE**

First results were achieved using silicon as a dopant [3]. In the following years, many dopants like Y, Al, Sr, La, Ge, N, etc. were successfully utilized to achieve ferroelectricity. Among the different variants, a special emphasis is on solid solutions of hafnium and zirconium since this material system makes a wide process window for the dopants possible, which results in an inherently stable process and also enables rather low annealing temperatures [4]. Since ferroelectricity is a material property that requires a crystalline structure (see fig. 1), typically an annealing step is carried out after the film deposition or more frequently even after top-electrode deposition. When comparing the properties of ferroelectric hafnium oxide with those of perovskite based ferroelectrics (Table I), the most striking differences are the very high coercive field and the low relative permittivity of HfO2.

It was confirmed in 2015 that the phase leading to ferroelectricity in hafnium oxide is the orthorhombic Pca21 phase [5]. This phase is not stable in bulk hafnium oxide. The exact mechanism of its stabilization in thin films is still a matter of intense research. Surface and interface energy have been proposed to play a major role. However, although experiments show the expected trends from such a model, there are also some important deviations. It has been recently

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| considered, | that | the | kinetic | | barrier | between | the |
| thermodynamically | | stable | | monoclinic, | | tetragonal, | and |

orthorhombic phases is important in avoiding the monoclinic phase, such that during cool down existing crystalline regions can be transformed from the tetragonal to the ferroelectric orthorhombic phase [6]. This understanding was substantiated by results from sputter deposited layers that showed that a higher oxygen content, leading to a higher fraction of monoclinic grains, can suppress the ferroelectricity in pure hafnium oxide while sputtering under oxygen deficient conditions can even help to make undoped hafnium oxide ferroelectric in a wide thickness range. Although these and related experiments help to get a basic understanding of the factors that need to be controlled to receive a high ferroelectric phase fraction, the complete understanding of the influences of doping, stress, oxygen content, surface energy and their interaction is still a topic of intense research.

|  |  |  |
| --- | --- | --- |
| 978-1-7281-4032-2/19/$31.00 ©2019 IEEE | 15.5.1 | IEDM19-354 |

**III.CAPACITOR BASED FERAM**

A natural way of utilizing the new possibilities given by the ferroelectricity in hafnium oxide is to replace the currently used perovskite based ferroelectric in a capacitor based FeRAM (fig. 2 a and fig. 3). However, like in DRAMs, a minimum charge is required to allow stable sensing during read (fig. 3c). Therefore, below the 90nm generation a DRAM-like stacked capacitor would be required. Attempts to realize 3D integration of PZT were not successful so far [7]. In contrast, the well-established atomic layer processes for HfO2 allow to easily integrate the material into a 3D stacked capacitor [8]. An alternative way was recently proposed using a 2T-1C cell where the capacitor is coupled to the gate of a read transistor (TR) and a second transistor (TP) is used to precharge the internal floating node SN (see fig. 4) [9]. In such an arrangement, the inherent amplification of the read transistor enables the sensing of very small switching currents, making the sensing of scaled capacitors possible (see fig. 5). However, for a device to challenge DRAM, unlimited endurance is necessary. In this respect the high fields in hafnium oxide based ferroelectrics, which are a consequence of the low layer thickness, paired with the high coercive field, becomes a major limiter. Although recently the understanding, and with this, the enhancement of the cycling endurance has increased (e.g. additional La doping can increase the endurance, see. Fig. 6), making it possible to foresee a cycling endurance of 1010 – 1012. However, unlimited endurance remains a severe challenge. Moreover, the unavoidable depolarization fields become more critical in the thin layer regime as can be seen from fig.7. Therefore, reliability needs careful optimization. An interesting alternative was proposed three years ago [10] using an antiferroelectric material combined with a built in bias field. Test capacitors that use this antiferroelectric RAM concept show improved cycling and imprint behavior.

**IV.FERROELECTRIC FIELD EFFECT TRANSISTOR**

When a ferroelectric is integrated into the gate stack of a MOS transistor, the VT of the device will depend on the polarization direction of the ferroelectric. This approach can overcome the scaling limitations of capacitor based ferroelectric memories since the inherent amplification of the transistor allows a constant charge per area rather than a constant absolute charge for proper sensing. Hafnium oxide is especially suited to realize ferroelectric field effect devices. The high coercive field allows for a reasonably sized memory window even in thin films and it also helps to stabilize the retention while the low permittivity reduces the depolarization field. Using such thin films, the material can be integrated into various existing and emerging transistor architectures as illustrated in fig. 8. Moreover, hafnium oxide is the standard gate dielectric in modern CMOS processes, and therefore, the integration into a CMOS process can be done with little process overhead [11]. Fig. 9 illustrates that a standard CMOS device can be integrated next to a FeFET device using the Globalfoundries 28nm FeFET process without deteriorating either the FeFET or the standard CMOS device performance. Full memory arrays show promising performance [11].

Therefore, realizing a low cost embedded nonvolatile memory is in reach. In scaled down devices, new effects are discovered which are attributed to the fact that small devices contain only a limited number of domains [12]. These, together with the possibility to integrate the FeFETs very close to other CMOS devices, open the path towards overcoming the von-Neumann bottleneck. When the stored information inside a FeFET is used as one input variable, calculations with this variable can be done without a memory access [13]. Such gates can be cascaded as shown in fig. 10. Moreover, the accumulative switching dynamics observed in scaled down devices can be utilized to realize the integrate-and-fire behavior of a neuron [14], while the continuous switching of larger devices allows one to realize the spike time dependent plasticity (STDP) of a synapse [15].

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| The | **V.** | **FERROELECTRIC TUNNEL JUNCTIONS** | | | | the |
| ferroelectric | | tunneling | junction | requires |

ferroelectric to be scaled down to a thickness in the 3nm range or below. Under conditions that are practically relevant for CMOS integration, this is a non-trivial task in hafnium oxide based ferroelectrics. However, when the ferroelectric is combined with a thin tunneling barrier, the switching and the tunneling can be decoupled to a certain degree [16,17] (see fig. 11 and fig. 12a)). A critical issue here is the low read current. Again, the circuit presented in fig. 4 could be an ideal fit. Fig. 12b shows first results of such an approach operating a FeFET in FTJ mode.

**VI.SUMMARY**

Ferroelectricity in hafnium oxide overcomes the CMOS integration challenges observed with perovskite ferroelectrics. The material innovation has brought a new phase of innovations to all three basic versions of ferroelectric memory devices: FeRAM, FeFET and FTJ.

ACKNOWLEDGMENT

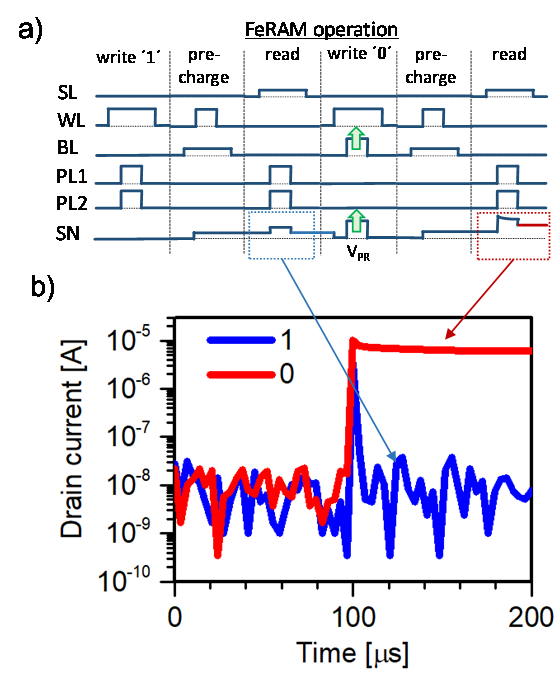
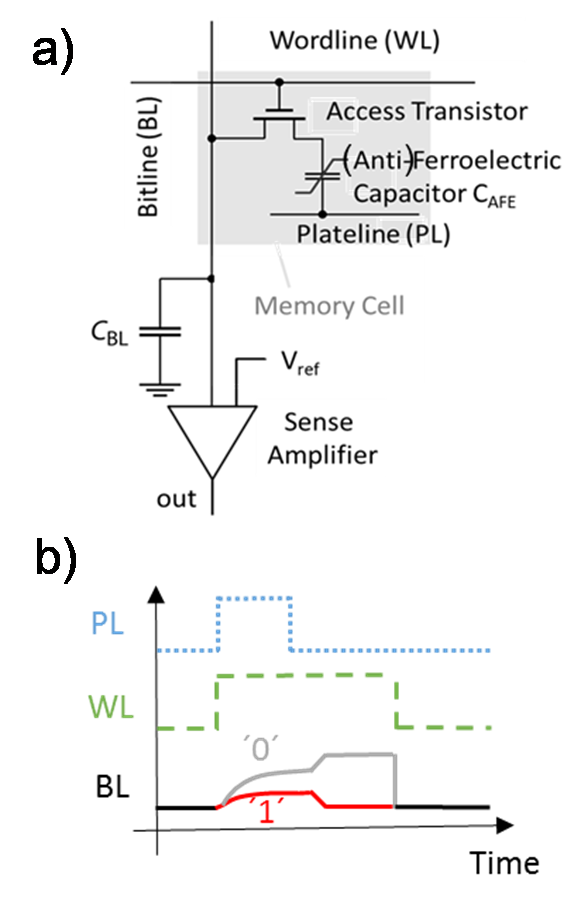
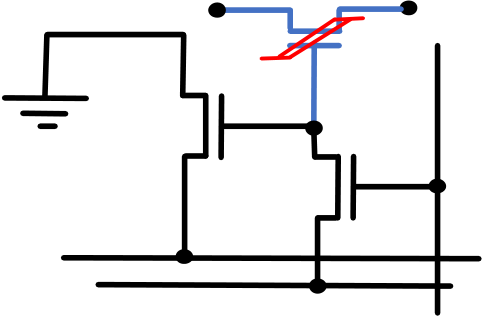
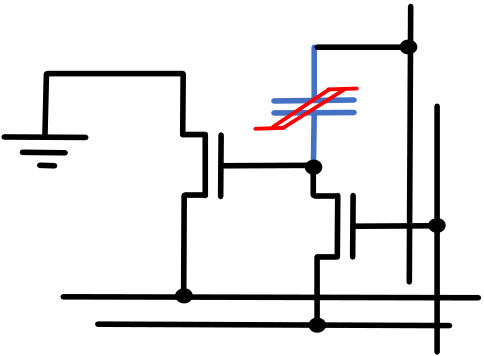
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| The | authors | gratefully | acknowledge | support | by |

GLOBALFOUNDRIES Fab1 LLC & Co. KG, Dresden, Germany. This work was financially supported by the European Fund for Regional Development EFRD, Europe supports Saxony, and by funds released by the delegates of the Saxon parliament and by the European Union’s Horizon 2020 research and innovation program under grant agreement No 780302.

REFERENCES

[1] K Prall, IEEE International Memory Workshop (IMW), pp 1-5 (2017)   
[2] C -U Pinnow and T Mikolajick, J Electrochem Soc 151, K13-K19 (2004) [3] T S Boescke et al , Appl Phys Lett 99, 102903 (2011)   
[4] J Mueller et al , Nano Lett 12, 4318-4323 (2012)   
[5] X Sang et al , Applied Physics Letters 106, p 162905 (2015)   
[6]M H Park et al , Advanced Electronic Materials 5 (3), 1800522 (2019)   
[7] J -M Koo et al , IEDM Techn Digest , 340-343 (2005)   
[8] J Muller et al , IEDM Techn Digest , pp 10 8 1-10 8 4 (2013)   
[9] S Slesazeck et al , International Memory Workshop (IMW), pp 1-4 (2019)   
[10] M Pesic et al , IEDM Techn Digest , pp 11 6 1-11 6 4 (2016)   
[11] S Duenkel et al , IEDM Techn Digest , pp 19 7 1 - 19 7 4 (2017)   
[12] H Mulaosmanovic et al , ACS applied mat & interf 9, 4, pp 3792-3798 (2017) [13] E T Breyer et al , IEDM Techn Digest pp 28 5 1-28 5 4 (2017)   
[14] H Mulaosmanovic et al , Nanoscale 10 (46), 21755-21763 (2018)   
[15] H Mulaosmanovic et al , Symposium on VLSI Technology, pp T176 - T177 (2017) [16] S Fujii et al , IEEE Symposium on VLSI Technology, pp 1-2 (2016)   
[17] B Max et al , Proceedings of ESSDERC, pp 142-145 (2018)

IEDM19-355 15.5.2



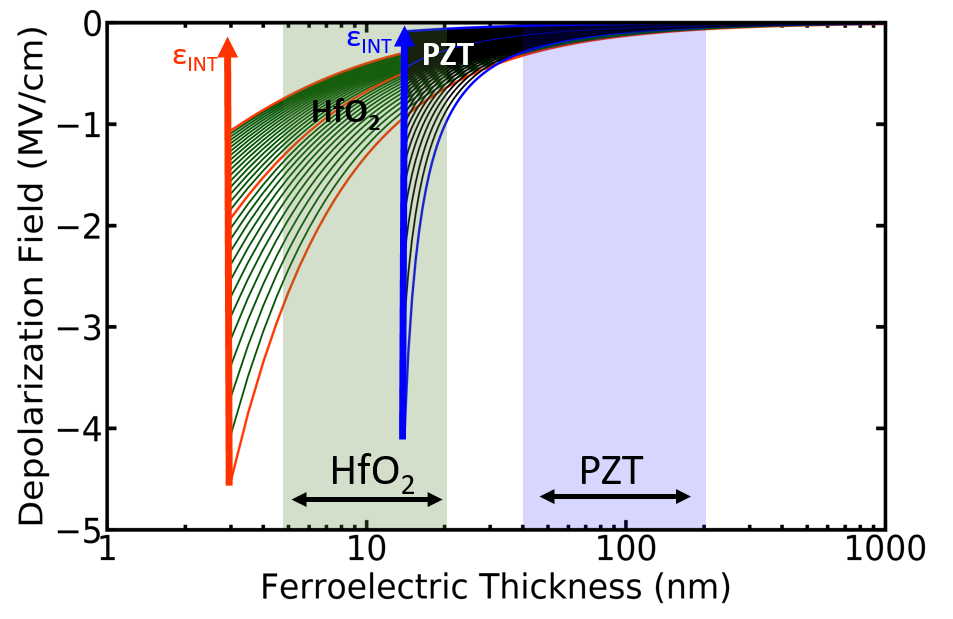
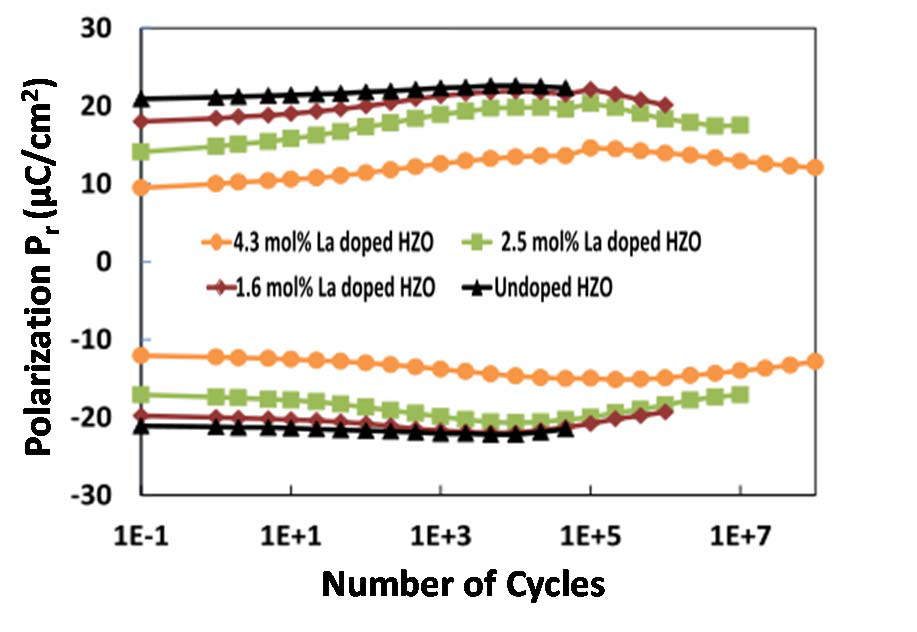
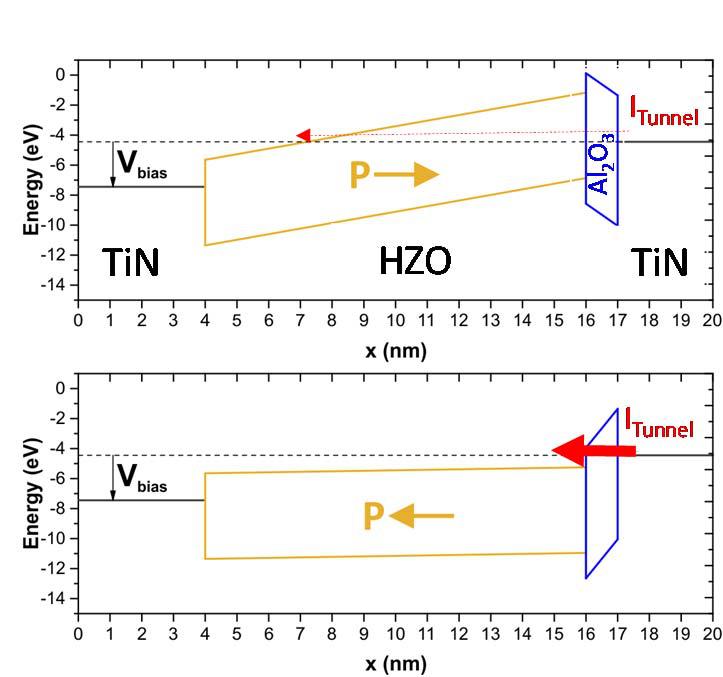
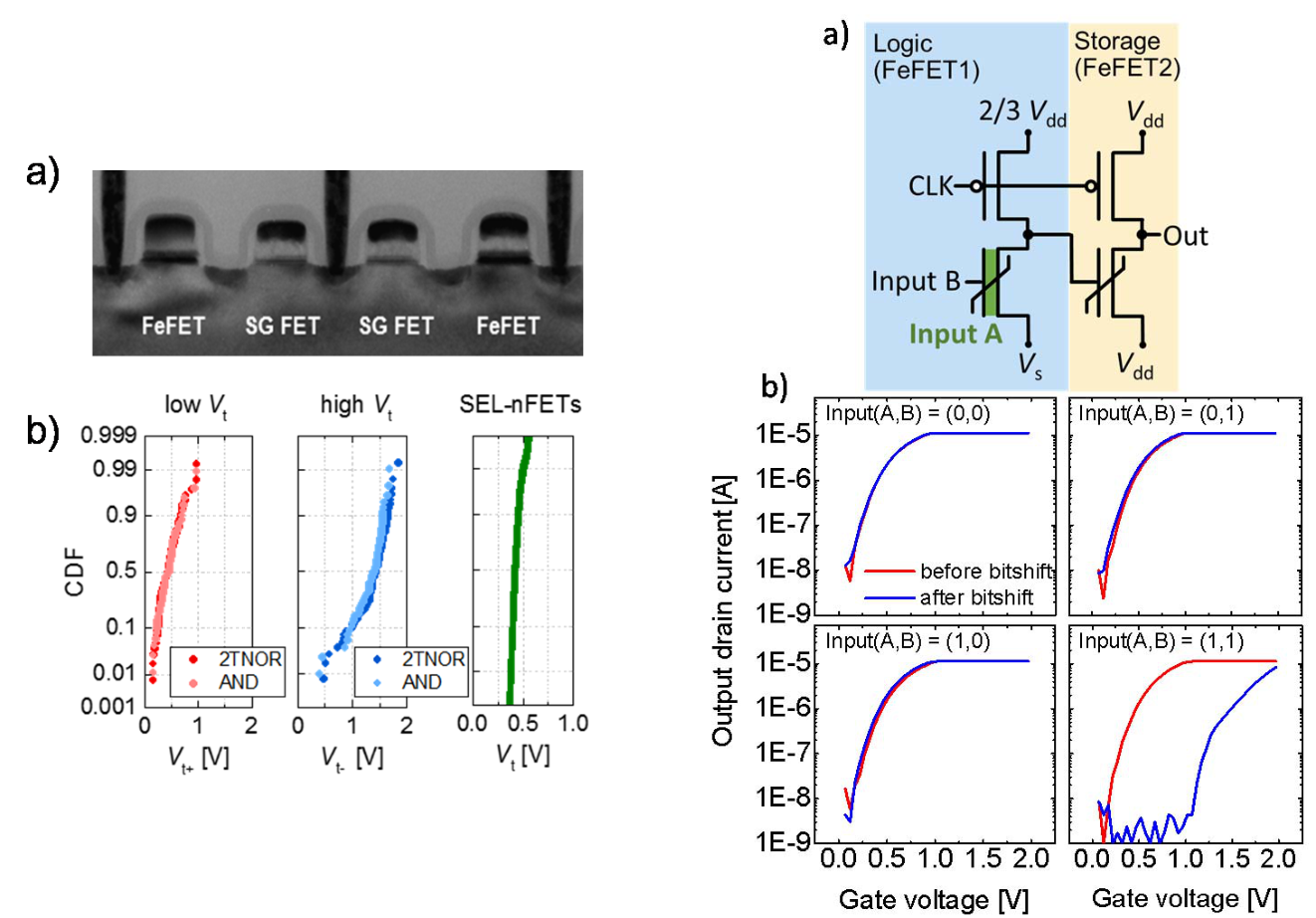
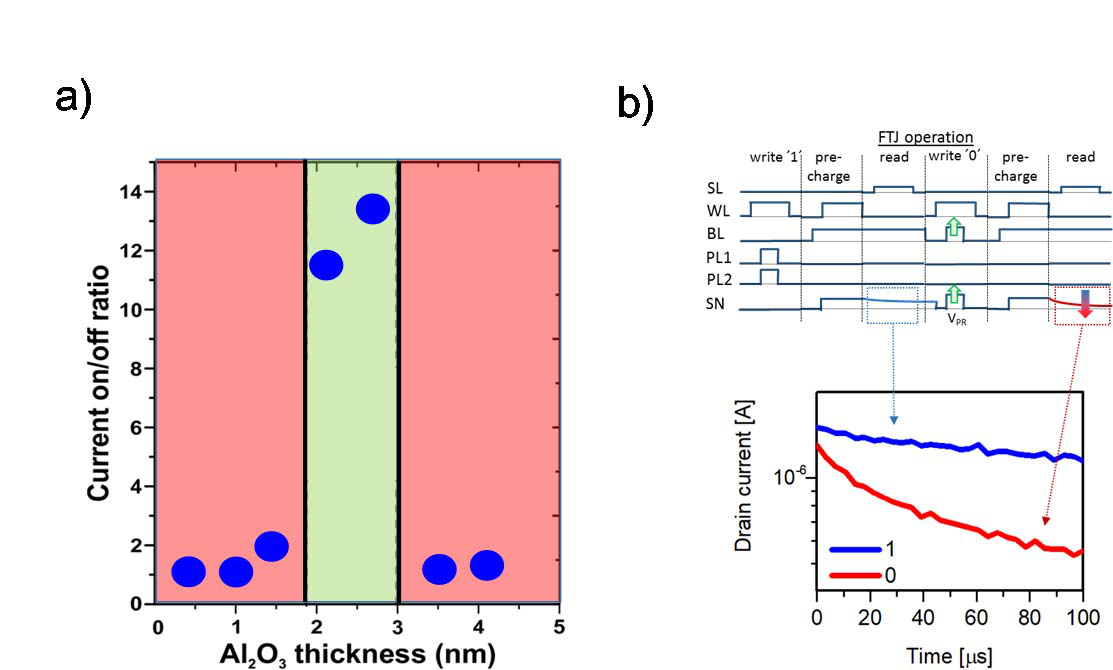
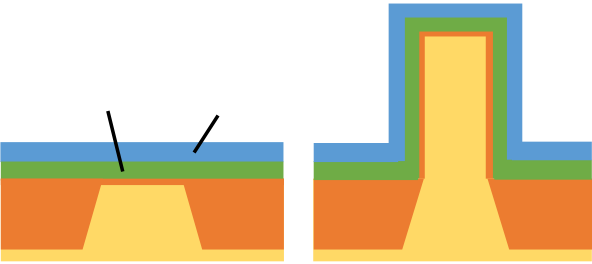
|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| a) |  | | | b) |  | | | | Tab. I. Important properties of the ferroelectric materials |
| doped hafnium oxide (X:HfO2) and lead zirconium titanate |
| (PZT). Note the pronounced differences in coercive field |
| and relative permittivity. |
| ABO3 | | | PZT | |  |  |  | | --- | --- | --- | |  | X:HfO2 | PZT (PbZrxTi1-xO3) | | coercive field EC in MV/cm | 0.8 - 2 | 0.1 | | switched charge (2PR) in µC/cm2 | 30-60 | 30-60 | | relative permitivity εr | 20-30 | 300-800 | |
| HfO2 | | |
|  | Hf4+ | |  | A2+ | Pb2+ | |
|  | O2- | O2- | |
|  | | O2- |
|  | B4+ | Zr4+ /Ti4+ | |

Fig. 1. Schematic of the crystal structure for (a) orthorhombic hafnium   
oxide and b) a typical perovskite of the general form ABO3. The arrows   
indicate the movement of the ions during ferroelectric switching. In today’s   
commercial nonvolatile memories the perovskite lead zirconium titanate   
(PZT) is the standard ferroelectric material used.

|  |  |  |
| --- | --- | --- |
| a) 1T/1C FeRAM | b) FeFET | c) FTJ |

WL

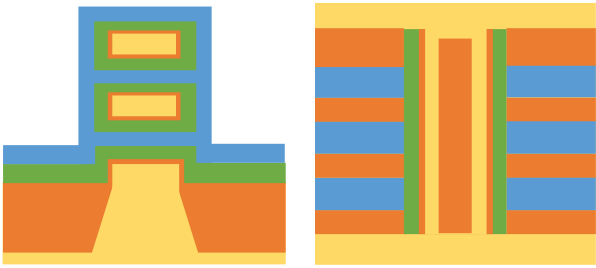
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| BL | |  | | BL | | WL | | | | WL | BL | | |
| PL | |  | | | |
| SL | |
| Fig. 2. Different options to realize a memory cell from a ferroelectric material. a) 1T/1C FeRAM cell. This cell resembles the cell of a dynamic random access memory with the capacitor dielectric replaced by the ferroelectric. b) Ferroelectric Field Effect Transistor (FeFET) cell. Here, the ferroelectric is used as the gate dielectric of a MOSFET. c) Ferroelectric Tunneling Junction (FTJ). In the FTJ, a very thin ferroelectric is used that allows tunneling and the tunneling current is modulated by the polarization of the ferroelectric | | | | | | | | | | | | | Fig. 3. a) FeRAM cell connected to wordline (WL), bitline (BL), plate line (PL) and sense amplifier. (b) Plate line (PL), wordline (WL) and bitline (BL) signals during read operation. |
| a) | PL | | | b) | | | PL1 | | PL2 | | | | |
| C1 | | | | TS | | | | | | | | | |
| TR | | | SN | TR | | | | SN | | | | | |
| TP | | | | TP | | | | | | | | | |
| BL | | | | SL | BL | | | | | SL | | | |
| WL | | | | WL | | | | | | | | | |
| Fig. 4. a) 2T-1C FeRAM cell. The read transistor TR provides the amplification to read the signal on the storage node SN. The precharge transistor TP allows to precharge the storage node to a defined level. b) Variant of the 2T-1C cell where the capacitor is realized by a ferroelectric field effect transistor. | | | | | | | | | | | | Fig. 5. a) Pulsing scheme and b) measurement results to demonstrate the feasibility of the 2T-1C concept in the implementation given in fig. 5b). | |
| 15.5.3 | | | | | | | | | | | | IEDM19-356 | |



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Fig. 6. Field cycling behavior of hafnium-zirconium films doped with significantly different lanthanum concentrations. The lanthanum doping can enhance the endurance. | | | | Fig. 7. Depolarization field in HfO2 and PZT as a function of film thickness, assuming a constant dead layer at the electrodes of 1nm and a range of relative permittivity values of the dead layer εINT. |
| a) | **Planar** | b) | **FinFET** |

Ferroelectric

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| c) | X:HfO2 | | Gate | | **3D NAND** |
| SiO2 | Si | | |
| **Nanosheet** | | | d) |



|  |  |  |  |
| --- | --- | --- | --- |
| Fig. 8. Different device architectures of FeFETs | Fig. 9. a) Hafnium oxide based FeFET | | Fig. 10. Two stage logic in memory operation. The |
| enabled by ferroelectric HfO2. a) Planar FeFET, b) | integrated next to a standard nFET. b) VT | |
| FeFET of the second stage is only switched when |
| ferroelectric FinFET, Ferroelectric nanowire or | distributions for low VT, high VT of the FeFET | |
| both the internal input A and the external input B |
| nanosheet transistor, and d) 3D NAND FeFET. | and standard nFET for devices integrated next | |
| of the first gate are at a logic ´1´ realizing a NAND |
| to each other (2TNOR) in comparison to | |
| function. |
| separated devices (AND). | |
| Fig. 11. Band diagram of two layer ferroelectric tunnel junction for the two possible polarization states. | | Fig. 12. (a) On/off current window of a two layer ferroelectric tunnel junction and (b) demonstration of FTJ operation in the 2T – 1 FTJ circuit shown in fig. 5b. | |

IEDM19-357 15.5.4